ABSTRACT

In an integrated decision feedback equalizer and clock and data recovery circuit one or more flip-flops and/or latches may be shared. One or more flip-flops and/or latches may be used in retiming operations in a decision feedback equalizer and in phase detection operations in a clock recovery circuit. Outputs of the flip-flops and/or latches may be used to generate feedback signals for the decision feedback equalizer. The output of a flip-flop and/or latches may be used to generate signals that drive a charge pump in the clock recovery circuit.

SDB/cah

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